

# Programmable Spike-Timing-Dependent Plasticity Learning Circuits in Neuromorphic VLSI Architectures

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Hardware implementations of spiking neural networks offer promising solutions for computational tasks that require compact and low-power computing technologies. As these solutions depend on both the specific network architecture and the type of learning algorithm used, it is important to develop spiking neural network devices that offer the possibility to reconfigure their network topology and to implement different types of learning mechanisms. Here we present a neuromorphic multi-neuron VLSI device with on-chip programmable event-based hybrid analog/digital circuits; the event-based nature of the input/output signals allows the use of address-event representation infrastructures for configuring arbitrary network architectures, while the programmable synaptic efficacy circuits allow the implementation of different types of spike-based learning mechanisms. The main contributions of this article are to demonstrate how the programmable neuromorphic system proposed can be configured to implement specific spike-based synaptic plasticity rules and to depict how it can be utilised in a cognitive task. Specifically, we explore the implementation of different spike-timing plasticity learning rules online in a hybrid system comprising a workstation and when the neuromorphic VLSI device is interfaced to it, and we demonstrate how, after training, the VLSI device can perform as a standalone component (i.e., without requiring a computer), binary classification of correlated patterns.

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## 1. INTRODUCTION

Artificial spike-based neural networks offer a promising paradigm for a new generation of brain-inspired computational models. A wide range of theoretical and computational models have already been proposed for both basic neuroscience research [Kempler et al. 1999; Gerstner and Kistler 2002] and practical applications [Belatreche et al. 2006; Rowcliffe and Feng 2008]. Neuromorphic *very large-scale integration* (VLSI)

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circuits represent an ideal technology for implementing these types of networks using hybrid analog/digital design techniques, and for building devices that have a very high potential in a wide range of applications such as pattern and data classification [Mitra et al. 2009; Giulioni et al. 2009; Schmuker et al. 2014], object recognition [Nere et al. 2012; Khosla et al. 2014], feature extraction [Vogelstein et al. 2007], and orientation selectivity [Choi et al. 2004; Chicca et al. 2007]. In particular, the main advantage of implementing these spiking neural networks in neuromorphic Very Large Scale Integration (VLSI) technology is their compactness and low power consumption, which are critical features when implementing large-scale neural architectures [Mead 1990; Moradi et al. 2013; Chicca et al. 2014; Azghadi et al. 2014b].

In these types of networks, synapses represent an essential component for signal processing, as they are at the same time the site of memory (they store the network's synaptic weight values), and play a fundamental role in computation (they implement crucial temporal and nonlinear dynamics). Synaptic weight values can be updated following the prescription of different types of learning algorithms that typically depend on the pre- and post-synaptic neuron activity [Abbott and Gerstner 2004; Brader et al. 2007; Graupner and Brunel 2012]. The different learning strategies have a profound effect on the post-synaptic neuron functionality and on the spiking neural network behavior [Laughlin and Sejnowski 2003]. Implementing such types of synapses and learning mechanisms in compact electronic systems is essential for developing efficient large-scale spiking neural networks and brain-inspired computing technologies [Azghadi et al. 2013a, 2014a]. However, as the implementation of the learning algorithm often depends on the specific application domain and on the nature of the data to process, it can be useful to develop compact electronic implementation of spiking neural networks in which the weights can be adjusted by off-chip learning algorithms (e.g., implemented on a workstation, micro-controller, or *field programmable gate arrays* (FPGA)).

In this article we demonstrate how it is possible to train a hardware spiking neural network using software-defined spike-based learning algorithms. We present a hybrid *software* (SW) *hardware* (HW) neural processing system that comprises a mixed signal analog/digital spiking neural network VLSI device interfaced to a workstation. The custom VLSI device comprises analog silicon neuron circuits [Indiveri et al. 2011], analog synaptic dynamics elements, and asynchronous digital event-based interfacing circuits for transmitting and receiving spikes. The device also integrates asynchronous digital programmable synaptic weight circuits for setting and changing the strengths of the silicon synapses with off-chip learning algorithms that can implement different types of spike-based synaptic plasticity rules [Pfister and Gerstner 2006; Brader et al. 2007; Clopath et al. 2010; Graupner and Brunel 2012]. The mixed signal analog/digital neural network device used in this work has already been described in detail in Moradi and Indiveri [2014]. Here we apply the device to spike-based learning problems, describing the details of the experimental setup required for controlling and programming the proposed neural device. We interface the device to a workstation and show how the hybrid SW-HW system can implement different types of spike-based learning algorithms online. Finally, after training a perceptron architecture, we demonstrate how the device can act as an efficient standalone binary classifier of correlated patterns, without requiring a workstation in the loop.

## 2. NEUROMORPHIC SPIKING NEURAL NETWORKS

The simulation of *spiking neural network* (SNN) on standard computers can be very onerous, requiring large amounts of memory and/or CPU time [Azghadi et al. 2014b]. Attempts are being made to speed up these simulations using *graphical processing unit* (GPU)-based approaches [Nageswaran et al. 2009; Fidjeland et al. 2009, 2013] or dedicated computing architectures [Furber et al. 2013]. Alternatively, full custom

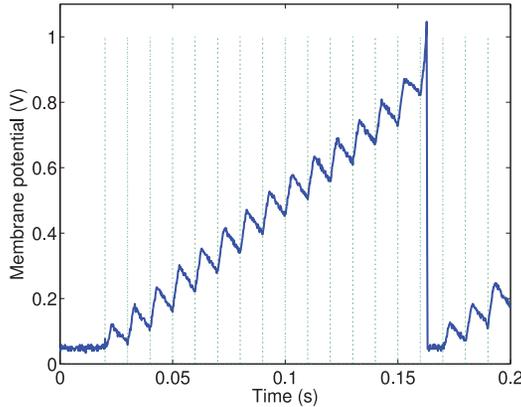


Fig. 1. Measured response of a silicon neuron (implementing a model of a leaky I&F neuron) being stimulated by a 100 Hz input spike train via an excitatory synapse.

VLSI implementations of spiking neural network can be implemented using dedicated analog, digital, or mixed signal analog/digital circuits. Examples of both fully digital [Arthur et al. 2012] and hybrid analog/digital [Schemmel et al. 2010; Moradi and Indiveri 2014] spiking neural network chips have been recently proposed. In these systems, spiking neurons are typically implemented as *integrate-and-fire* (I&F) models [Koch 1999] which collect all of the signals (typically, currents) produced by the synapses, and produce a spike event when the integrated sum exceeds a threshold. The equation governing the neuron’s subthreshold dynamics, for example, in the case of a leaky Integrate-and-Fire (I&F) model neuron [Gerstner and Kistler 2002], is given by

$$\tau \frac{d}{dt} u(t) = -u(t) + RI(t), \quad (1)$$

where  $\tau$  is the leaky integrator time constant,  $1/R$  represents the neuron leak conductance, and  $I(t)$  represents the total synaptic input current. Synaptic currents are produced by the neuron’s synapses when they get stimulated by the input spikes. Figure 1 shows an example of the response measured from a silicon neuron being stimulated via an input excitatory synapse with a regular input spike train of 100 Hz.

Synapses also typically have first-order dynamics, but they can have both linear and nonlinear response properties. In all cases, however, their response is proportional to their synaptic weight. Learning occurs by adapting the synaptic weights of all the synapses afferent to a neuron, following the prescription of the specific learning rule considered. In these types of neural network, the “source” neurons produce spikes and transmit them to synapses of other “destination” neurons. Depending on the network structure (e.g., multilayer feed-forward architectures, recurrent architectures, etc.), different types of computational models can be implemented [Dayan and Abbott 2001]. Information is processed through the propagation of spikes and the generation of the weighted synaptic responses in the network [Gerstner and Kistler 2002]. It is widely believed that learning, computation, and memory processes take place in synapses [Sjöström et al. 2008]. Since the learning and computation in an SNN comprise a dynamic process, the synapses should also be dynamic and modifiable. However, the open question is how these modifications take place in the synapses within the brain, and how they can lead to network properties that allow the system to carry out robust and real-time computation so efficiently and accurately. Although there is no general agreement as to the answer to this question, there are several hypotheses stating that

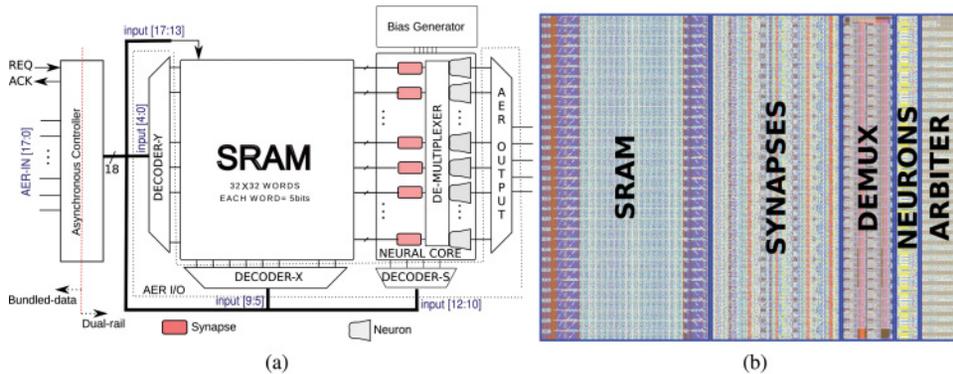


Fig. 2. IFMEM chip block diagram: (a) The device comprises a neural-core module with an array of synapses and integrate-and-fire neurons, an asynchronous SRAM module to store the synaptic weight values, a bias generator to set the parameters in the analog circuits, and asynchronous control and interfacing circuits to manage the AER communication; (b) layout picture comprising the SRAM, neural-core, and AER output blocks. In particular, the layout of the SRAM block measures  $524 \times 930 \mu\text{m}$ , the synapse array measures  $309 \mu\text{m}$  in length, the synapse de-multiplexer measures  $132 \mu\text{m}$ , the neuron array  $60 \mu\text{m}$ , and the output AER arbiter  $105 \mu\text{m}$ .

these modifications take place in relation to the activity of pre- and post-synaptic neurons connected to the synapse [Sjöström et al. 2008]. These hypotheses that govern the synaptic weight changes are so-called synaptic plasticity models [Mayr and Partzsch 2010].

Due to the variety of neuron, synapse, and synaptic plasticity models, and because of different spiking neural network structures, it is essential to develop programmable neural network architectures such as the one presented in this work device, so as to explore the role of different spike-based learning rules and different neural network structures.

### 3. THE IFMEM CHIP

The multi-neuron chip used in this work is characterized by the fact that it comprises circuits that implement models of I&F neurons, as well as a programmable memory for storing the synaptic weights. Therefore, we will refer to this device as the IFMEM chip. The IFMEM chip was fabricated using a standard  $0.35 \mu\text{m}$  *complementary metal oxide semiconductor* (CMOS) VLSI technology and fully characterized in Moradi and Indiveri [2014]. It implements a neural network of 32 adaptive exponential I&F neuron circuits [Indiveri et al. 2011] with dynamic synapse circuits. The IFMEM chip makes use of the *address-event representation* (AER) protocol to receive and transmit events that represent input and output spikes, respectively.

A block diagram of the chip architecture is shown in Figure 2(a). All circuits on the chip that implement the neural and synapse dynamics are in the “neural core” block. The neuron circuits are implemented using an adaptive exponential integrate-and-fire model [Brette and Gerstner 2005; Indiveri et al. 2010], while the parts of those synapse circuits responsible for integrating input spikes and producing temporal response properties that have biologically plausible time constants are implemented using a *differential pair integrator* (DPI) circuit [Bartolozzi and Indiveri 2007]. Depending on the input address event, different types of synapse dynamics can be triggered: excitatory with slow time constants (e.g., to emulate NMDA-type synapses), excitatory synapses with faster time constants (e.g., to emulate AMPA synapses), or inhibitory synapses (e.g., to emulate GABA-type synapses). Since the DPI can be used as a linear low-pass filter, it is possible to make use of a single integrator circuit for any of the synapse dynamics

considered (e.g., NMDA, AMPA, or GABA) and to multiplex it in time to integrate the contributions from multiple spiking inputs (e.g., via multiple SRAM cells), thus saving precious silicon real-estate.

The analog components of these circuits have programmable bias parameters that can be set with an on-chip 32-bit temperature-compensated programmable bias generator [Delbruck et al. 2010]. The synaptic weights of the synapses are stored in a  $32 \times 32$  5-bit digital SRAM block, designed with asynchronous circuits for interfacing to the AER components. The digital weight values are converted into currents with an on-chip *digital-to-analog converter* (DAC), so that the addressed synapse circuits produce *excitatory post-synaptic current* (EPSC) with amplitudes proportional to their weights. Thanks to the synapse time-multiplexing scheme, the total number of synapses that a neuron sees is equivalent to the total number of SRAM cells present in each row. The SRAM cells can work in “feed-through” mode or in storage mode. In feed-through mode, input events contain both the address of the destination SRAM cell and the synaptic weight bits, and the synapses generate Excitatory Post Synaptic Current (EPSC) online as data is received. In storage mode, the input events contain only the address of the destination SRAM cell, and the weight bits used by the synapses are the ones stored in the addressed SRAM cell [Moradi and Indiveri 2011]. Therefore it is possible to interface the device to a workstation and use it in feed-through mode to train the spiking neural network online with all of the Hardware (HW) components in the loop, eventually storing the final synaptic weight matrix in the SRAM block at the end of the training phase. Once the training has completed, it is possible to use the device in standalone mode without requiring a PC in the loop, and use the stored weights to carry out the learned task.

Figure 2(b) shows a section of the layout of the IFMEM chip comprising the main blocks described before. As shown, each block is extremely compact, so it is possible in principle to scale up the network to very large sizes (e.g., a chip fabricated using an inexpensive  $0.35\mu\text{m}$  technology, using a relatively small area of  $55\text{mm}^2$ , would implement a network of 512 neurons and 256k synapses, each having 5-bits precision.

In Figure 3 we show an example of a simple spiking neural network architecture that can be formed using the IFMEM chip by using its silicon neurons, integrator synapses, and SRAM cells. The SRAM cells that act as virtual synapses keep the synaptic weights and can be updated according to any desired spike-based learning algorithm. A neuron in the proposed architecture, shown in Figure 2(a), can be stimulated by up to  $32 \times 32 \times 4 = 4096$  virtual synapses thanks to the de-multiplexing scheme available on the proposed neuromorphic architecture [Moradi and Indiveri 2014]. The post-synaptic neuron generates spikes when its integrated input currents, that is, those EPSCs generated by its related synapses, exceed a predetermined threshold. At this time, the neuron generates an action potential and its membrane potential is then reset to a controllable reset potential [Indiveri et al. 2011].

## 4. THE HARDWARE-SOFTWARE NEUROMORPHIC SYSTEM

### 4.1. Experimental Setup

The experimental setup, shown in Figure 4, consists of three main components: a Linux PC, a generic AER interface, and the neuromorphic hardware. The PC is used to control and interact with the neuromorphic system. It generates input spike trains (AER input) and transfers them to the IFMEM chip via an AER interface. The PC also monitors, records, and analyzes the AER output of the chip. Via a separate channel, the PC also sends bias values to the IFMEM chip, which control its various circuit parameters.

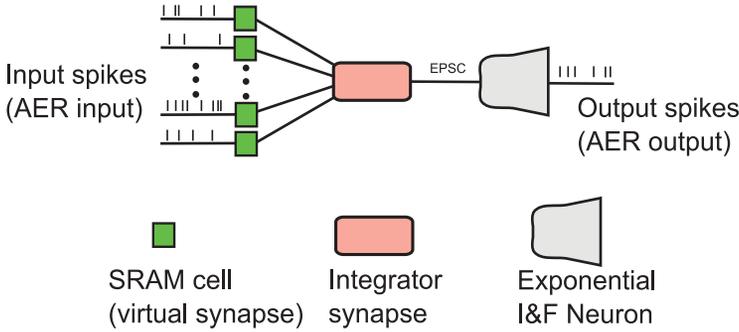


Fig. 3. A simple spiking neural network architecture implemented on the proposed neuromorphic device shown in Figure 2(a). The input spikes are integrated by a physical synapse that acts as an integrator. The synapse generates EPSC proportional to input firing rate, and the synaptic weights stored on the SRAM cells, through on-chip programmable DACs. The generated EPSC will cause the silicon neuron to fire spikes if its membrane potential exceeds the spiking threshold. A similar structure has been used in all of the experiments presented in this article.

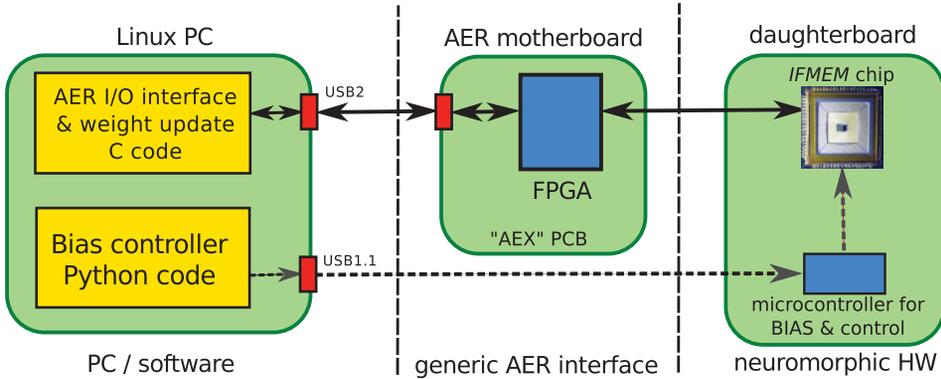


Fig. 4. Experimental setup of the hardware-software neuromorphic system. Dashed lines represent the control path for setting analog parameters and configuring the IFMEM chip, and solid lines represent the path for the address-events dataflow (from and to the IFMEM chip).

Figure 5 shows two printed circuit boards that host the three main hardware components of the system (shown in Figure 4), including an FPGA, a micro-controller, and the IFMEM neuromorphic chip. The PCB shown on the left is the AER motherboard, the so-called AEX board, which contains the FPGA. Directly attached to the AEX board is a daughter-board containing the IFMEM chip and the micro-controller. The AEX board is a generic AER communication platform derived from the board first presented in Fasnacht et al. [2008]. It consists of a high-speed (480 MHz) USB2.0 interface and a Field Programmable Gate Array (FPGA) device. The USB interface enables the FPGA to communicate bi-directionally with the PC attached. The FPGA receives spike trains from the PC via USB and then generates them accordingly on its parallel AER output interface to stimulate the IFMEM chip. Vice versa, the FPGA monitors the AER output of the IFMEM chip: each address event received by the FPGA is sent to the PC, together with a 128ns-resolution timestamp of when exactly the spike was received at the parallel AER input of the FPGA. The AEX board also contains a high-speed serial AER interface to communicate with other AEX boards. Since only one such board is required in the single-chip experimental setup described, the serial AER interface was not used.

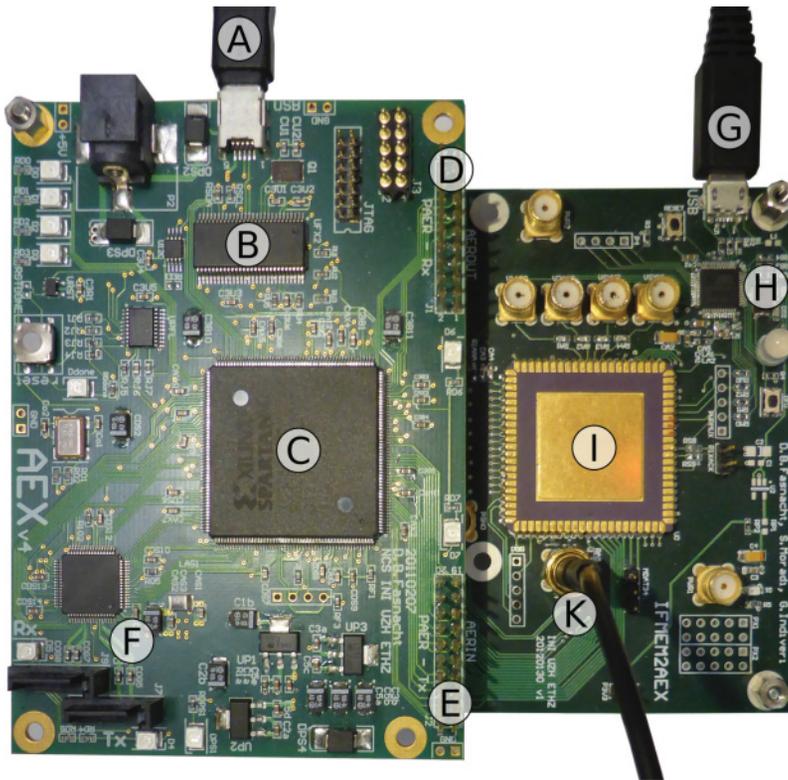


Fig. 5. The AEX printed circuit board with the attached daughter-board carrying the IFMEM chip: (A) high-speed USB interface for AER communication; (B) USB interface chip; (C) FPGA for AER monitoring and sequencing; (D) parallel AER interface (chip to FPGA); (E) parallel AER interface (FPGA to chip); (F) serial AER section (unused); (G) full-speed USB interface for IFMEM bias control; (H) micro-controller for bias control; (I) the IFMEM chip; (K) analog voltage output connection.

Directly attached to the AEX communication board is a daughter-board. Figure 5 shows the two boards together. The daughter-board contains both the IFMEM chip and the circuitry needed to support the chip, such as voltage regulators and connectors to measure analog output voltages generated by the chip. It also contains a simple micro-controller that includes a full-speed (12 MHz) USB interface. Via this second USB interface, the PC sends the bias values to the micro-controller. The micro-controller then programs the on-chip bias generator circuits to set the circuit bias voltages to values specified by the user.

#### 4.2. Programming the Neuromorphic System

As shown in Figure 4, the synaptic plasticity weight updates, the AER I/O interfacing, as well as the bias controlling are all programmed in software on the Linux PC in the neuromorphic setup. In order to form a spiking neural network with a specific synaptic plasticity rule on this setup, several steps need to be taken. The first step is to calibrate the silicon neurons, synapse integrators, and the programmable DACs in the IFMEM chip using an automated routine (developed in Python). This calibration routine on the host PC can access the IFMEM chip via a micro-controller hosted on the IFMEM chip daughter-board, and can interface to the PC via a USB port. The parameters changed on the IFMEM chip, via the calibration routine, control the behaviors of the neural

components (including the response properties of silicon neurons and the dynamics of integrator synapses) on the neuromorphic device. The calibration process is useful to determine the parameters for setting desired properties of the neural network, such as membrane time constants, learning rates, etc.

In a second step, after calibration, the PC uses the AEX board to transfer the input spike trains to the chip, and at the same time records those AER addresses that correspond to the post-synaptic spikes being generated by the neurons on the chip. Each AER input (pre-synaptic event) contains four slots of information, including 18 bits as shown in Figure 2(a). These bits describe different specifications, including:

- the address of the post-synaptic neuron (5 bits);
- the address of the SRAM block containing the required synaptic weight (5 bits);
- the type (either inhibitory or excitatory) and the address of the desired physical synapse (3 bits); and
- the desired digital value for the synaptic weight that will be written to the addressed SRAM block (5 bits).

Each post-synaptic event (AER output), however, only shows the address of the post-synaptic neuron that generated an event (spike).

In the third step, the recorded input (pre-synaptic) and output (post-synaptic) spikes are timestamped and represented as an address event (AE) with a time resolution of  $1\mu\text{s}$ . This data is then fed to a software module which implements a specific spike-based learning rule such as STDP. This module, implemented in C language in our setup, then calculates the required synaptic weight changes depending on the spike timings of various pre- and post-synaptic neurons, and uses this information to update the 5-bit synaptic weights stored in the related SRAM cells of the IFMEM chip. As the chip produces post-synaptic spikes (in response to the inputs arriving to the chip, and as a function of the learned synaptic weights), the system continues to learn in an online feed-through mode.

When learning is not required anymore, the system can be set to storage mode. In this mode the synaptic weights cannot be updated anymore and the chip can be used as a standalone device (i.e., disconnected from the PC) to receive input spikes from external sensory devices (e.g., from an event-based sensory VLSI device [Liu and Delbruck 2010]), process them according to its synaptic weights, and generate output spikes in result.

## 5. EXPERIMENTAL RESULTS

In this section we demonstrate how the device can be used in a hybrid SW-HW system to implement different forms of spike-based plasticity. In particular, we demonstrate that the IFMEM chip can work with both standard *spike-timing-dependent plasticity* (STDP) learning prescriptions as well as with the more elaborate ones that are being proposed in the computational neuroscience literature [Gjorgjieva et al. 2011; Clopath et al. 2010; Graupner and Brunel 2012]. In addition, we demonstrate how the specific variants of Spike-Timing Dependent Plasticity (STDP) that we use can reproduce the properties of the Bienenstock-Cooper-Munro (BCM) rate-based learning rule [Bienenstock et al. 1982]. Before implementing any synaptic plasticity rules on the IFMEM chip, first we characterize the response properties of available silicon neurons and programmable synapses.

### 5.1. Silicon Neuron and Programmable Synapse Response Properties

The silicon neurons and programmable synapses available on the IFMEM chip should be first calibrated to respond correctly to the input stimuli. In order to calibrate the chip parameters, we first injected constant current in the neuron circuit and adjusted the

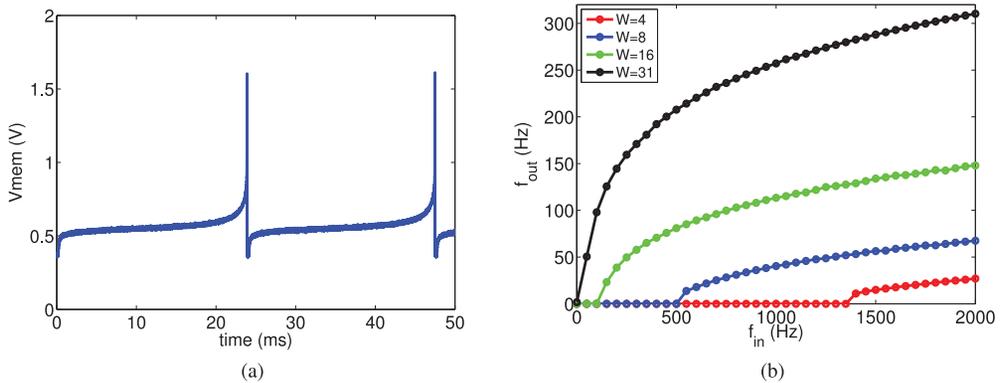


Fig. 6. Neuron and synapse characterization: (a) Silicon neuron membrane potential in response to constant current injection; (b) output neuron frequency versus frequency of incoming spikes, representing either a very high firing rate of a single source or multiple sources at lower firing rates.

silicon neuron parameters to obtain biophysically realistic response properties with biologically realistic time constants (see Figure 6(a)). Furthermore, to calibrate the synapse parameters, we first adjusted the parameters of those on-chip Digital to Analog Converters (DACs) that convert the SRAM bits into analog subthreshold currents, then we stimulated the synapse with regular spike trains at different frequencies, and measured the neuron response. Since the synapse is configured to behave as a linear filter, we stimulated a single synapse with input frequencies as high as 2000 Hz to represent inputs from many neurons at lower frequencies (by means of the superposition principle). Figure 6(b) shows the response of a silicon neuron to these input spike trains for different synaptic weight values. As shown, we calibrated the on-chip DACs to set synaptic weights that have a low gain, even for the highest weight value ( $w = 31$ ). As stated earlier, the DAC parameters for the synapse, as well as the silicon neuron parameters, were set using a software module implemented on the PC to control the on-chip bias generator circuit [Delbruck et al. 2010], via a micro-controller, integrated on the host *printed circuit board* (PCB) (see Figure 5).

Note that the high input spiking rates are not biologically plausible for single synapses (which typically receive spikes with rates in the order of tens of Hertz or less). These inputs, however, are meant to represent the spikes arriving from multiple sources (e.g., a 2KHz input spike train could represent spikes arriving from 2000 different neurons, each spiking at 1 Hz). This is possible thanks to the linear properties of the synapse integrator circuit, which can therefore exploit the super-position principle to collect low-rate spikes arriving from multiple “virtual” synapses into a single high-rate integration node. In addition to demonstrating the ability of the circuits to process high input firing rates, we have shown in a previous study that these silicon neurons and synapses can operate correctly also with biologically realistic times and firing rates [Azghadi et al. 2013d].

## 5.2. Competitive Hebbian Learning through STDP

The STDP learning rule has been widely used in many computational studies [Song et al. 2000] as well as multiple VLSI implementations [Bofill-I-Petit and Murray 2004; Indiveri 2002; Bamford et al. 2012; Azghadi et al. 2013a, 2014b]. The basic STDP rule is expressed as

$$\Delta w = \begin{cases} \Delta w^+ = A^+ e^{\left(\frac{-\Delta t}{\tau_+}\right)} & \text{if } \Delta t > 0 \\ \Delta w^- = -A^- e^{\left(\frac{\Delta t}{\tau_-}\right)} & \text{if } \Delta t \leq 0, \end{cases} \quad (2)$$

where  $\Delta t = t_{\text{post}} - t_{\text{pre}}$  is the timing difference between a single pair of pre- and post-synaptic spikes. According to this model, the synaptic weight will be potentiated if a pre-synaptic spike arrives in a specified time window ( $\tau_+$ ) before the occurrence of a post-synaptic spike. Analogously, depression will occur if a pre-synaptic spike occurs within a time window ( $\tau_-$ ) after the post-synaptic spike. These time windows are not usually longer than about 50ms. According to Eq. (2), the magnitude of potentiation/depression will be determined as a function of the timing difference between pre- and post-synaptic spikes, their temporal order, potentiation and depression time constants, and their relevant amplitude parameters ( $A^+$  and  $A^-$ ).

It has been shown that changes in synapses trained by the basic STDP learning mechanism lead eventually to a bi-modal distribution in which synapses are either strongly potentiated or strongly depressed. This behavior has been described as “competitive Hebbian learning” [Song et al. 2000]. In particular, the bi-modal distribution arises when: (i) the weight of individual synapses is bounded and (ii) on average, synapses tend to be more depressed than potentiated (e.g.,  $A^+ \tau_+ < A^- \tau_-$  in Eq. (2), when the area under the STDP curve for LTP and LTD are compared).

Here, we reproduce the competitive Hebbian learning behavior in our system by configuring a network composed of a single I&F neuron connected to its 32 5-bit digital synapses. We demonstrate how, when governed by STDP, the synaptic weights diverge into two distinguished groups over time.

The experiment is summarized as follows: We initialize the system by injecting a small constant current to one silicon neuron to increase its excitability, and by setting all the weights of its 32 input synapses to their mid value of  $w = 16$ . Next, we apply 32 independent Poisson spike trains with firing rates of 50 Hz to all these 32 synapses. The weighted EPSCs produced by the synapses are integrated by the silicon neuron, which eventually produces spikes and transmits them as address events to the workstation using the AER protocol. The timing of the post-synaptic spikes (measured from the HW) and of the pre-synaptic spikes (synthesized in Software (SW)), applied to each of the 32 synapses, is then used to update the values of the 5-bit weights stored in the synapse-corresponding SRAM cells, following an SW algorithm that implements the rule of Eq. (2). The SW algorithm first measures the  $\Delta t$ s among the pre-synaptic spikes from various synapses and the post-synaptic spikes and then, according to the STDP learning rule shown in Eq. (2) and its parameters, computes and returns the magnitude of the weight changes for all 32 synapses connected to the neuron. The STDP parameters used for this experiments are:  $A^+ = 0.5$ ,  $A^- = 0.527$ , and  $\tau_+ = \tau_- = 20\text{ms}$ . Please also note that during all synaptic plasticity experiments presented in this article, the nearest-neighbour spike interaction model (as opposed to the all-to-all spike interaction) is utilised.

Figure 7 shows how the synaptic weights evolve over time to reach a stable state in which they show the expected bi-modal distribution. Note how we were able to reproduce the competitive Hebbian learning behavior even with weights bounded to 5-bit resolution, and with hybrid SW-HW spike-timing interactions.

### 5.3. Implementing BCM through STDP

Although Bienenstock Cooper Munro (BCM) is an inherently rate-based rule and depends on the activities of pre- and post-synaptic neurons, recent studies have shown that a timing-based triplet STDP learning rule can reproduce BCM-like functionality [Gjorgjieva et al. 2011]. Here we demonstrate how this rate-based functionality can be realized by our SW-HW system by using the triplet STDP learning rule [Gjorgjieva et al. 2011] to update the 5-bit synaptic weight values of the IFMEM chip.

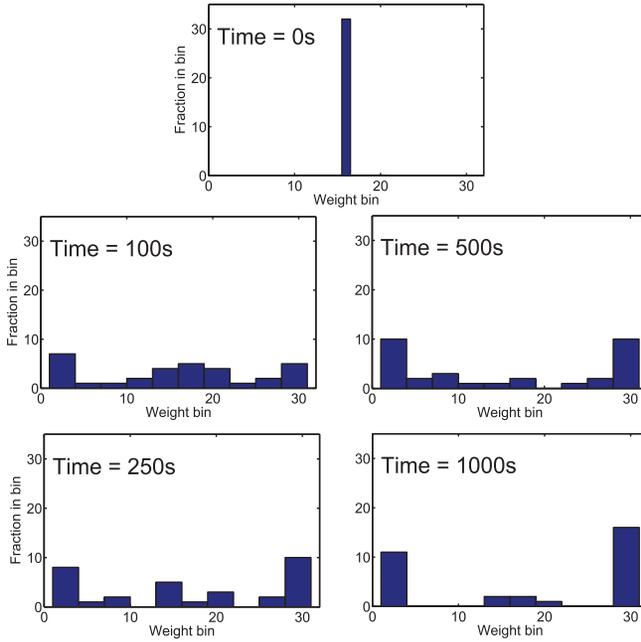


Fig. 7. Synaptic weights evolve to reach an equilibrium state when modified by the STDP learning rule. Here, 32 synaptic weights (weight bins), each with 32 digital states, are altered by STDP over time. The top figure shows that all 32 synaptic weights are set to 16 in the beginning at time = 0s, that is, the fraction of weights in weight bin 16 is 32. The other figures show the evolution of weights over time to reach a steady state at time = 1000s. The synaptic weights stay almost fixed thereafter, and the post-synaptic neuron firing rate held in an almost direct relation to the mean firing rate of pre-synaptic spike trains, that is, 50 Hz.

The triplet-based STDP can be formulated as

$$\Delta w = \begin{cases} \Delta w^+ = e^{\left(\frac{-\Delta t_1}{\tau_+}\right)} \left( A_2^+ + A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)} \right) \\ \Delta w^- = -e^{\left(\frac{\Delta t_1}{\tau_-}\right)} \left( A_2^- + A_3^- e^{\left(\frac{-\Delta t_3}{\tau_x}\right)} \right), \end{cases} \quad (3)$$

where  $\Delta w = \Delta w^+$  for  $t = t_{\text{post}}$  and if  $t = t_{\text{pre}}$  then the weight change is  $\Delta w = \Delta w^-$ .  $A_2^+$ ,  $A_2^-$ ,  $A_3^+$  and  $A_3^-$  are potentiation and depression amplitude parameters,  $\Delta t_1 = t_{\text{post}(n)} - t_{\text{pre}(n)}$ ,  $\Delta t_2 = t_{\text{post}(n)} - t_{\text{post}(n-1)} - \epsilon$  and  $\Delta t_3 = t_{\text{pre}(n)} - t_{\text{pre}(n-1)} - \epsilon$ , are the time differences between combinations of pre- and post-synaptic spikes. Here,  $\epsilon$  is a small positive constant which ensures that the weight update uses the correct values occurring just before the pre- or post-synaptic spike of interest, and finally  $\tau_-$ ,  $\tau_+$ ,  $\tau_x$  and  $\tau_y$  represent time constants [Pfister and Gerstner 2006].

It has been shown [Pfister and Gerstner 2006] that, for Poisson-distributed spike trains, Eq. (3) can be approximated as

$$\langle dw/dt \rangle = -A_2^- \tau_- \rho_{\text{pre}} \rho_{\text{post}} - A_3^- \tau_- \tau_x \rho_{\text{pre}}^2 \rho_{\text{post}} + A_2^+ \tau_+ \rho_{\text{pre}} \rho_{\text{post}} + A_3^+ \tau_+ \tau_y \rho_{\text{post}}^2 \rho_{\text{pre}}, \quad (4)$$

where  $\rho_{\text{pre}}$  and  $\rho_{\text{post}}$  represent the mean firing rates of the pre- and post-synaptic spike trains, respectively.

Generally, BCM theory suggests that the synaptic weight changes are in a linear relationship with the pre-synaptic, and a nonlinear relationship with the post-synaptic mean firing rates [Bienenstock et al. 1982]. Therefore a general description of the BCM

rule can be written as

$$dw/dt = \rho_{pre} \cdot \phi(\rho_{post}, \theta), \quad (5)$$

where  $\phi$  is a function that satisfies the conditions  $\phi(\rho_{post} > \theta, \theta) > 0$ ,  $\phi(\rho_{post} < \theta, \theta) < 0$  and  $\phi(0, \theta) = 0$ . Essentially, if the post-synaptic firing rate  $\rho_{post}$  is below the threshold  $\theta$ , then  $dw/dt$  is negative and the synaptic weight is depressed. Conversely, the synaptic weight is potentiated if the post-synaptic firing rate is larger than the threshold  $\theta$ , and it is left unchanged if  $\phi = 0$ , that is, if  $\rho_{post} = \theta$  [Pfister and Gerstner 2006].

Eqs. (4) and (5) can be mapped together if two conditions are satisfied. The first condition requires having a linear relationship between the pre-synaptic firing activity ( $\rho_{pre}$ ) and the synaptic weight change ( $(dw/dt)$ ), as shown in Eq. (5). This condition is satisfied if  $A_3^- = 0$  in the triplet STDP equation (Eq. (4)). This will lead to a minimal version of the *triplet spike-timing-dependent plasticity* (TSTDP) rule presented in Pfister and Gerstner [2006], which has been shown to account for various synaptic plasticity neuroscience experiments, including those dealing with higher-order spike trains [Wang et al. 2005]. The second condition requires that the sliding threshold  $\theta$ , that determines the frequency in which depression turns to potentiation, is proportional to the expectation of the  $p^{th}$  power of the post-synaptic firing rate ( $\rho_{post}$ ) [Pfister and Gerstner 2006; Bienenstock et al. 1982]. This second condition can be satisfied if the threshold of the BCM rule is defined as

$$\theta = \langle \rho_{post}^p \rangle (A_2^- \tau_- + A_2^+ \tau_+) / \rho_0^p A_3^+ \tau_+ \tau_y. \quad (6)$$

Given this equation, the sliding threshold effect of the BCM rule is proportional to the post-synaptic firing rate, with the proportionality factor set by the STDP rule parameters.

To implement BCM via the triplet STDP rule in the IFMEM chip setup, we used a single synapse connected to a post-synaptic silicon neuron and changed its efficacy using the STDP rule of Eq. (3). At the beginning of the experiment, the initial weight of the synapse is set to its maximum value of 31. This high synaptic weight makes the post-synaptic neuron fire at a high rate proportional to the pre-synaptic firing rate [Azghadi et al. 2013b]. The SW pre-synaptic spike train and the spike train produced by the silicon neuron are then used to calculate the amount of weight changes in the corresponding synaptic efficacy according to a minimal model of triplet STDP [Gjorgjieva et al. 2011].

Figure 8 shows the total amount of weight changes in response to Poisson spike trains of 20s length for a range of pre-synaptic spike rates from 0 Hz up to 100 Hz. In this figure, the sliding threshold feature of the BCM learning rule is regenerated through changing the amount of one of the parameters of the TSTDP learning rule, that is,  $A_3^+$ . According to Eq. (6), with increase in the  $A_3^+$  parameter, the threshold decreases and slides toward lower postsynaptic firing rates. Please note that in the presented experiment, the silicon neuron parameters, as well as the synaptic weight parameters in its corresponding physical synapse, that is, the differential pair integrator, are calibrated in a way that pre- and post-synaptic neurons are in a relatively linear relationship [Moradi and Indiveri 2014; Azghadi et al. 2013b]. In this figure, each data point corresponds to the mean of the weight changes over 10 trials, and the error bar represents the standard deviation of the weight change over these trials. This amount of weight changes can then be discretized and written back into the SRAM. The STDP parameters that have been used in this experiment are  $A_3^- = A_2^+ = 0$ ,  $A_2^- = 0.0068$ ,  $\tau_+ = 16.8\text{ms}$ ,  $\tau_- = 33.7\text{ms}$ , and  $\tau_y = 114\text{ms}$ .

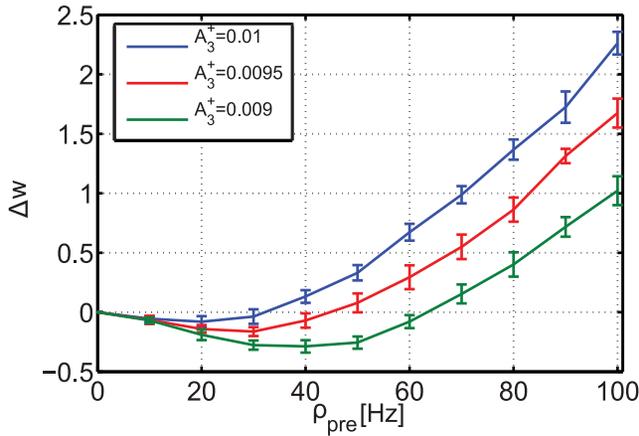


Fig. 8. The sliding threshold feature of the rate-based BCM rule is replicated through the triplet STDP rule implemented on the IFMEM chip.

#### 5.4. Classification of Complex Correlated Patterns

Here we use the TSTDTP learning rule, with its parameters tuned for exhibiting BCM behavior (see Figure 8), to demonstrate how the proposed VLSI device can perform classification of binary patterns with high levels of correlation.

The neural classifier implemented is composed of one neuron and 30 synapses which are arranged in a single-layer perceptron-like architecture. The goal is to train the perceptron synaptic weights via the Triplet Spike-Timing Dependent Plasticity (TSTDTP) algorithm to learn to distinguish two input patterns, UP and DOWN, in an unsupervised fashion. After training, the HW perceptron should be able to respond with a high firing rate to pattern UP, and with a low one to pattern DOWN. This is a similar experimental scenario to the semi-supervised learning scenario utilized in a similar classification task using spiking neural networks [Giulioni et al. 2009].

The two UP and DOWN patterns can have various degrees of correlation. The correlation determines the amount of overlap in the input synapses used as well as the similarity in the output response of the neuron: when there is no correlation, one pattern is applied to 15 random synapses and the other to the remaining 15 synapses (no overlap).

The pattern UP stimulates 15 synapses with Poisson spike trains that have a high mean firing rate of 300 Hz, while pattern DOWN comprises 15 Poisson spike trains with a low mean firing rate of 20 Hz. Therefore, in the case of zero correlation, the two patterns are likely to produce different outputs (depending on the values of the synaptic weights) even before learning. However, for the case of nonzero correlations, a random subset of  $N$  input synapses are always stimulated by high mean firing rate spike trains of 300 Hz, while the rest of the synapses are assigned to the two UP and DOWN patterns. For instance, if the number of correlated synapses is 10, then 10 randomly synapses are stimulated by Poisson spike trains of 300 Hz, and the remaining 20 synapses will be reserved for the UP and DOWN patterns. In this case, because of the  $N$  common high input synapses, the two patterns will have closer mean firing rates and therefore their classification becomes more challenging. Therefore, in the beginning of the learning phase, the output frequency range of the perceptron cannot be distinguished between the two patterns and, as a result, learning is required to classify the two patterns.

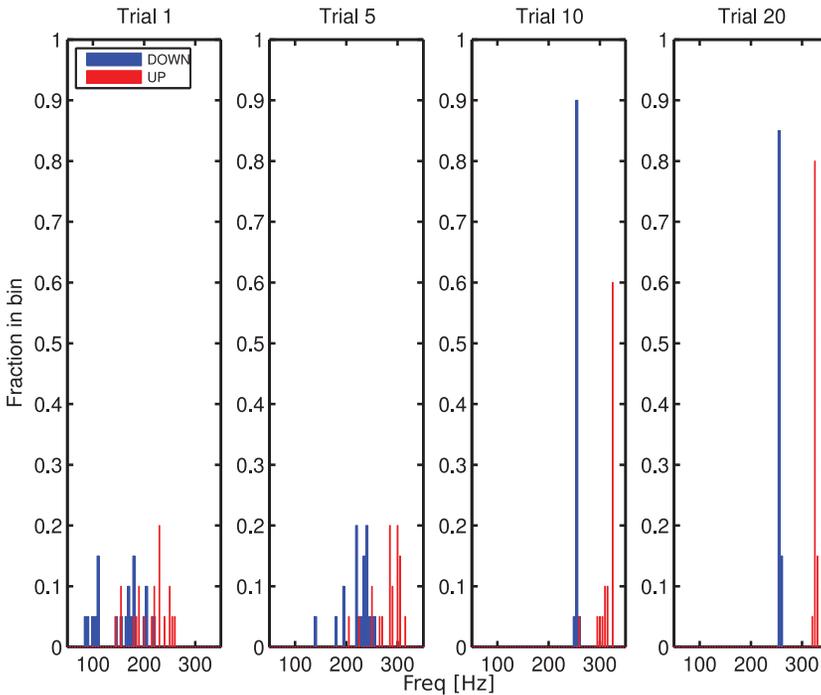


Fig. 9. Distribution of the neuron output frequencies during different stages of learning. In the beginning of the learning phase, when initial weights are random, the neuron cannot distinguish between the two patterns. During the learning trials, the synapses are being modified and the neuron begins to effectively discriminate between the two patterns from trial 20. In this experiment the correlation is equal to 20 %, that is, there are 6 inputs that are common to the two patterns that always receive high firing rates.

The training phase is composed of several trials. In each trial, one of the two patterns UP or DOWN is randomly applied to the 30 input synapses with a set degree of correlation and with a new distribution of Poisson spikes. The two patterns have equal probability to be selected. For each trial, the synaptic weights are modified according to the TSTDTP. In our experiment the synaptic weights reach a steady state and do not change significantly after about 20 trials, in which the input spike trains lasted 10s each.

Figure 9 shows how the distribution of the neuron output firing rates changes with learning after 1, 5, 10, and 20 trials. The output neuron rates were collected over 20 classification runs, with each run comprising 20 learning trials and 20% correlation. In each run, the synaptic weights are initialized to random 5-bit values, the definition of UP and DOWN patterns is changed, and a new random order of UP and DOWN patterns applied across trials is defined.

As expected, the TSTDTP learning rule used tends to decrease the weights of those synapses targeted by the DOWN pattern, while it tends to increase the weights of both the UP and correlated (overlapping) synapses. After learning, the neuron will therefore fire with high firing rates when stimulated with UP patterns, and with low ones when stimulated by DOWN patterns. While after a few trials (e.g., see second and third panels of Figure 9) the neuron already performs above chance levels, many trials (20 in our experiments) are required to unambiguously classify the two patterns.

This classification performance is robust and holds also for large amounts of correlation (up to 90 %) in the input patterns. In terms of classification accuracy, we consider

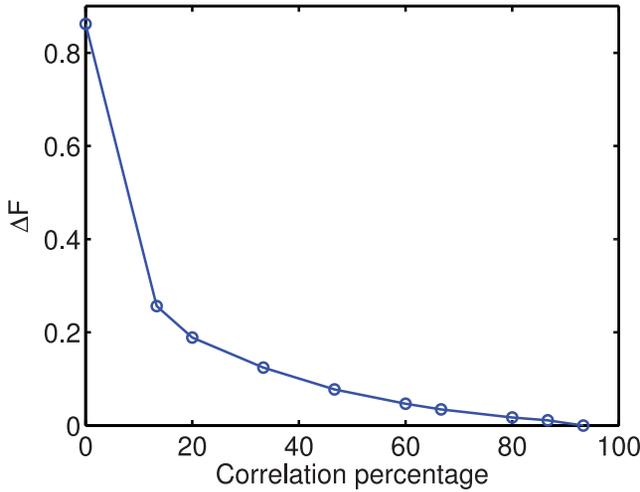


Fig. 10. The performance of the classifier implemented on the IFMEM chip. Here  $\Delta F = (F_{UP}^{min} - F_{DOWN}^{max}) / F_{UP}^{min}$ , where  $F_{UP}^{min}$  and  $F_{DOWN}^{max}$  are the minimum and maximum frequencies for pattern UP and DOWN, respectively, for all 20 runs at the end of learning in trial 20.

a DOWN pattern correctly classified if the neuron output frequency is less than a set threshold in response to this pattern; and similarly, an UP pattern is correctly classified if the neuron response to such pattern has a firing rate higher than the threshold. In our experiments the classifier has 100% correct performance, even with correlation levels of 87% (i.e., 26 overlapping synapses) if the classification threshold is adaptive (e.g., if it is set just below the minimum frequency in response to the UP patterns). What changes, however, is the difference in responses to the two patterns. Figure 10 shows how this difference decreases as the correlation among the input patterns increases.

Although the developed classification device demonstrates promising results in the targeted classification scenario, its ability in more challenging pattern classification tasks has yet to be evaluated in future research.

## 6. CONCLUSIONS

We presented a hybrid SW-HW neuromorphic system that utilizes a previously developed programmable neuromorphic VLSI device (IFMEM chip) that comprises silicon neurons and event-driven synapses with programmable synaptic weight circuits. We demonstrated how this device can be used in the developed system to implement different types of spike-timing-dependent plasticity learning rules, and demonstrated how these rules can reproduce interesting competitive Hebbian learning and rate-based behaviors, even with the limitations of the hardware implementation (5-bit resolution for the weights, mismatch of the analog subthreshold circuits, etc.). Finally, we described how the hybrid SW-HW learning setup proposed can be used to train a perceptron to perform binary classification in an unsupervised way, and to be robust to extremely high correlations in the input patterns.

The device and setup proposed therefore represent a useful real-time low-power computing platform for exploring the effectiveness of different types of spike-based learning algorithms, validating their performance at runtime on real-time custom analog/digital hardware, and implementing robust perceptron-like neural network to carry out real-time classifications tasks. If the task can be solved after training the weights of the neural network, without requiring continuous or online training, then the platform proposed represents a standalone compact and low-power alternative to standard

full-digital computing solutions (no PC is required in the loop). The use of the AER representation for receiving inputs, computing with spikes, and transmitting signals in output makes this device an ideal computational platform for building embedded neuromorphic event-based computational systems that process events generated by neuromorphic sensory systems [Liu and Delbruck 2010].

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